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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,902	08/02/2001	Masahiko Watanabe	35.C15650	4530

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EXAMINER	
NGUYEN, LAM S	
ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 01/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/919,902	Applicant(s) WATANABE, MASAHIKO
	Examiner LAM S NGUYEN	Art Unit 2853

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosur Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 107 (FIG 11). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: In page3, line 19, symbol 108 can not denote an inverter circuit (See Fig 11). Appropriate correction is required.

Claim Objections

3. Claim16 objected to because of the following informalities: Page 33, line 13, the term "the above recoding" is not defined. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 3, 4, 7/1, 7/2, 7/3, 7/4, and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshino (JP020011873A) in view of Sato (U.S. 5734280).

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4).

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Hoshino does not disclose that the CPU generates a signal in accordance to the initialization completion signal.

However, Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to include such a signal because such a signal insures the proper operation of the circuit blocks being initialized as is designed by Hoshino and Sato.

5. Claims 5, 6, 7/5, and 7/6 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280) as regarded to claims 1, 2, 3, 4, 7/1-4, and 17, and further in view of Wong (U.S.5801561)

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Hoshino and Sato do not disclose the solution to solve the case that when any circuit block has not been initialized yet after a predetermined period passes.

However, Wong teaches that if a circuit block that has not been sufficient initialized, then that circuit block is asserted by an enable signal (in term or "a substitute reset signal") (Fig. 2) to start the initialization process.

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to include such a solution that an enable signal initializes any circuit block that has not been initialized after the predetermined period passes because such a solution insures to complete the initialization process of all circuit blocks in a certain period of time as is designed by Hoshino and Sato in view of Wong.

6. Claims 8/1-4 and 9/7/1-4 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280) as regarded to claims 1, 2, 3, 4, 7/1-4, and 17, and further in view of Mitani (U.S.5929672)

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Hoshino and Sato do not disclose the one-chip configuration of the integrated-circuit apparatus.

However, Mitani discloses a one-chip integrated-circuit apparatus (in term of "microcomputer") that including a CPU and circuit blocks (Column 4-5, line 63-6 and Fig. 4, element 20).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to constitute a CPU and circuit blocks in one chip because the one-chip configuration saves space, lessens cost for manufacturing, and decreases time for signal propagation and data processing as is designed by Hoshino and Sato in view of Mitani.

7. Claims 8/5-6 and 9/7/5-6 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280), Wong (U.S.5801561) as regarded to claims 5, 6, and 7/5-6, and further in view of Mitani (U.S.5929672)

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Wong teaches that if a circuit block that has not been sufficient initialized, then that circuit block is asserted by an enable signal (in term or "a substitute reset signal") (Fig. 2) to start the initialization process.

Hoshino, Sato, and Wong do not disclose the one-chip configuration of the integrated-circuit apparatus.

However, Mitani discloses a one-chip integrated-circuit apparatus (in term of "microcomputer") that including a CPU and circuit blocks (Column 4-5, line 63-6 and Fig. 4, element 20).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to constitute a CPU and circuit blocks in one chip because the one-chip configuration saves space, lessens cost for manufacturing, and decreases time for signal propagation and data processing as is designed by Hoshino, Sato, and Wong in view of Mitani.

8. Claims 10/1-4, 11/7/1-4, 14, 15, and 16 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280) as regarded to claims 1, 2, 3, 4, 7/1, 7/2, 7/3, 7/4 and 17, and further in view of Morita (U.S.6033050).

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Hoshino and Sato do not disclose the use of the integrated-circuit apparatus to initialize the control circuit and the driving circuit of an ink-jet recording apparatus of a printer.

However, Morita discloses the initialization of a printing head drive of a control circuit of an ink-jet printer at a frequency that depends on a kind of the printing head and printing method (Column 6, lines 49-54, and FIG. 4, element S15).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to use this integrated-circuit apparatus in an ink-jet printer for initializing the driving circuit and the control circuit because such an integrated-circuit apparatus insures the operation of the driving circuit and the control circuit is initialized with parameters set by the CPU as is designed by Hoshino and Sato in view of Morita.

9. Claims 10/5-6 and 11/7/5-6 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280), Wong (U.S.5801561) as regarded to claims 5, 6, and 7/5-6 and further in view of Morita

(U.S.6033050).

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Wong teaches that if a circuit block that has not been sufficient initialized, then that circuit block is asserted by an enable signal (in term or "a substitute reset signal") (Fig. 2) to start the initialization process.

Hoshino, Sato, and Wong do not disclose the use of the integrated-circuit apparatus in a printer.

However, Morita discloses a printer including a CPU and circuit blocks (FIG. 5).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to use this integrated-circuit apparatus in a printer for driving or controlling the operation of the print head because this integrated-circuit apparatus insures the operation of the driving circuit and the control circuit is initialized with parameters set by the CPU as is designed by Hoshino, Sato, and Wong in view of Morita.

10. Claims 12/8/1-4 and 13/9/7/1-4 rejected under 35 U.S.C. 103(a) as being

unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280), Mitani (U.S.5929672) as regarded to claims 8/1-4 and 9/7/1-4 , and further in view of Morita (U.S.6033050).

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Mitani discloses a one-chip integrated-circuit apparatus (in term of "microcomputer") that including a CPU and circuit blocks (Column 4-5, line 63-6 and Fig. 4, element 20).

Hoshino, Sato, and Mitani do not disclose the use of the integrated-circuit apparatus in a printer.

However, Morita discloses a printer including a CPU and circuit blocks (FIG. 5).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to use this integrated-circuit apparatus in a printer for driving or controlling the operation of the print head because this integrated-circuit apparatus insures the operation of the driving circuit and the control circuit is initialized with parameters set by the CPU as is

designed by Hoshino, Sato, and Wong in view of Morita.

11. Claims 12/8/5-6 and 13/9/7/5-6 rejected under 35 U.S.C. 103(a) as being unpantentable over Hoshino (JP020011873A) in view of Sato (U.S.5734280), Wong (U.S.5801561), Mitani (U.S.5929672) as regarded to claims 8/5-6 and 9/7/5-6, and further in view of Morita (U.S.6033050).

Hoshino's invention discloses:

an apparatus including a CPU, circuit blocks (Fig 1, elements 2,3,4)

an initialization completion signal (in the term of "an initialization success/failure signal" (1d) to show the success or failure of the initialization process (See Solution))

the initialization success/failure signal is transmitted from the circuit blocks to the CPU through a logic circuit (Fig.2, element 4)

Sato discloses an enable signal (in term of "an activation signal") generated when a signal is feedbacked from circuit blocks (Column 8, line 39-54). Also, Sato teaches the enable signal may be generated after a certain period (Column 5, line 61-65).

Wong teaches that if a circuit block that has not been sufficient initialized, then that circuit block is asserted by an enable signal (in term or "a substitute reset signal") (Fig. 2) to start the initialization process.

Mitani discloses a one-chip integrated-circuit apparatus (in term of "microcomputer") that including a CPU and circuit blocks (Column 4-5, line 63-6 and Fig. 4, element 20).

Hoshino, Sato, Wong, and Mitani do not disclose the use of the integrated-circuit apparatus to initialize the control circuit and the driving circuit of an ink-jet recording apparatus of a printer.

However, Morita discloses a printer including a CPU and circuit blocks (FIG. 5).

Therefore, it would have been obvious to one having ordinary skill in the art would be motivated to use this integrated-circuit apparatus in a printer for driving or controlling the operation of the print head because this integrated-circuit apparatus insures the operation of the driving circuit and the control circuit is initialized with parameters set by the CPU as is designed by Hoshino, Sato, and Wong in view of Morita.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lam Nguyen whose telephone number is (703) 305-3342. The examiner can normally be reached on Monday-Friday (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow, can be reached on (703) 308-3126. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722. Any inquiry or general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LN LN

December 31,2001

John Barlow
Supervisory Patent Examiner
Technology Center 2800